Adnan Kabbani

A'Sharqiyah University,
Ibra, Sultanate of Oman
Tel: +968 25401195
Cell: +968 91379517
Email: kabbani_a@hotmail.com, kabbani_a@asu.edu.om

NATIONALITY

Canadian

EDUCATION

Royal Military College of Canada, Kingston, ON, Canada

Ph.D., VLSI, 1999 - 2004

- Determined the optimum level of Intellectual Property (IP) blocks' development from re-usability and predictability point of view in Ultra Deep Submicron (UDSM) technology environment, as well as investigated the impact of target technology library-cells on the IP block design performance.
- Developed technology-portable models to predict cell-timing characteristics such as transition time and delay of complex CMOS gates.
- Developed transistor-sizing guidelines for area and delay optimization that can be used with virtual library synthesis.
- Thesis title: Timing driven IP block design methodology with emphasis on reusability.

Concordia University, Montreal, QC, Canada

M.Sc., VLSI, 1996 - 1999

- Investigated noise generation in high-speed dynamic CMOS systems and determined the noise immunity of such systems under various switching scenarios, and input transition times.
- Modeled the Simultaneous Switching Noise (SSN) and predicted the shape and the peak value of the SSN waveform.
- Thesis title: Modeling noise effects on dynamic CMOS circuits.

Damascus University, Damascus, Syria

B.Eng., Electronic, 1983 – 1988

- Five year engineering program
- Major of electronic engineering

York University, Toronto, ON, Canada

Project Management, Short Course, May, 2003

- Studied the principles for effective project management
- One week course

WORK EXPERIENCE

A'Sharqiyah University (ASU), Oman, Ibra, 2013- now

Department of Electronics and Communication Engineering, Associate Professor since 2016

Head of Electronics and Communication Engineering Department, July 2021-now

1. Manage the daily work of the department
2. Prepare course offering
3. Chair department meetings
4. Manage the teaching load of the faculty members
5. Propose the department budget
6. Submitted annual reports to Dean about the activities of the department
7. Evaluate the faculty performance

Chair of the University Research and Enterprise Committee (UREC) 2017-2018

1. Developed and reviewed the research strategy and systems to ensure excellence in research, innovation, training and knowledge transfer.
2. Evaluated and approve research projects/ training and visits and monitor and follow up the same in accordance with the rules.
3. Developed and reviewed policies, procedures and regulations governing all research activities including the policies on research ethics, biosafety and IP at ASU.
4. Proposed and allocated the budget for research activities at ASU.
5. Took measures to enhance and monitored the quality of ASU's research performance and research facilities/environment.
6. Initiated the means of research cooperation and collaboration with universities /research centers/industries outside the university at the national and international level.
7. Prepared annual report on the research activities at ASU.
8. Prepared annual Operational plan for UREC

Acting Dean, College of Engineering August 2015 - August 2016

- Supervised the good handling of daily work of the college
- Coordinated among the different departments of the college and with other units of the University
- Submitted recommendations with regard to the requirements of the college of a personnel, facilities, equipment, materials, books and other requirements
- Evaluated the performance of the teaching staff, researchers, technicians, and administrators
- Developed proposals with regard to the budget of the college
- Submitted annual reports to the Deputy Vice Chancellor on the progress of work and all activities of the college

Taught undergraduate courses

- *Digital Systems*
- *Circuit Theory I*
- *Circuit Theory II*
- *Electronic I*
- *Electronics II*
- *Digital Electronics*
- *CMOS Circuits Design*
- *Communication Electronics*
- *Power Electronics*
- *Renewable Energy*

Services to ASU

Committee commitments

- **Chair** of the University Research and Enterprise Committee (UREC), 2017-2018
- **Member** University Academic Board 2015-16, 2017 -2018 and 2021-now
- **Chair** The College Academic Board 2015-2016.
- **Member** of many other committees at the college and program levels

Other services

- Developed the operational plan for the college of engineering
- Developed the 4x4 program for Electronics and Communication Department
- Prepared job descriptions

Al-Wadi International University (WIU), Syria, Homs, Wadi Al Nadara, 2010- 2013

Head of Computer and Telecommunication Engineering Department 2011-2013

Taught undergraduate courses

- *Electronic circuit I*
- *Electronic circuit II*
- *Circuit Theory.*
- *Computer Arithmetic.*
- *Computer Architecture*
- *Discrete Mathematics*

Supervising undergraduate students

- Different projects in the area of microelectronics such as sensing and displaying ECG signal, and temperature measurement and controlling.

Services to WIU

- **Head** of Computer and Telecommunication Engineering Department
- Revised the Computer and Telecommunication Engineering Department
- Managed the teaching load of the faculty members
- Chaired search committees to shortlist and interview candidates for faculty member positions
- Managed the daily work of the department and other tasks assigned by the dean

Ryerson University, Toronto, ON, Canada

Assistant Professor, 2004 -2010

Taught graduate and undergraduate courses

- *Digital CMOS VLSI Integrated Circuits* (A graduate course)
- *Direct Study Course (EE8601)* (A graduate course)
- *Electronic Circuits I*
- *Electronic Circuits II*.
- *Low Power Integrated Circuits*.
- *Biomedical Instrumentation*.

Research and graduate students

- ***Research areas***
    - Power consumption modeling in complex CMOS gates; low power

implementation techniques targeting biomedical applications; noise modeling and effect on CMOS circuits; design for reusability and solar systems (recently)

- ***Supervised graduate students***
  - Completed: Three MASc. and two MEng. students

MASc. thesis titles

- Area-delay driven library-free synthesis
- High level FPGA implementation of adaptive signal segmentation and autoregressive modeling techniques
- On-chip interconnects modeling and timing driven buffer insertion

MEng. project titles

- Design and Implementation of portable and configurable RISC processor architecture
- Proposed implementation of various imaging modes of Optical Coherence Tomography (OCT) on FPGA

Service to Ryerson University

- **Stream Coordinator,** Undergraduate Microsystems Stream
- **Research Group Coordinator**, Computer Systems Engineering (CSE) research group
- **Member**, Electrical and Computer Engineering (ELCE) Graduate Student Admission Committee
- **Member**, Undergraduate Curriculum Committee
- **Member**, The Awards Committee
- **Member**, Graduate Scholarship Committee
- **Chair and Examiner,** Many M.Sc., and Ph.D. oral and written exam committees

CMC Microsystems, Kingston, ON, Canada

SoC Engineer, 2000 - 2004

- Led a project to develop a design flow for soft Intellectual Property (IP) blocks.
- Led a project to develop an application note for memory-core integration.
- Supported the Virage memory compiler and assisted other SoC activities such as developing platform microprocessor selection criteria and a technology roadmap.

Royal Military College of Canada, Kingston, ON, Canada

Teaching Assistant 1999-2004

- Assisted students with basic electrical theory.
- Developed tutorials for the Xilinx FPGA Foundation tool.
- Assisted students in Xilinx FPGA Foundation and Cadence Virtuoso CAD tools.

Concordia University, Montreal, QC, Canada

Research Assistant, 1997 - 1999

- Modeled noise immunity of dynamic CMOS circuits considering short-channel MOSFETs, and signal and clock inputs.
- Modeled simultaneous switching noise in CMOS circuits considering switching and quiet gates.

Homs Sugar Company, Homs, Syria

Electrical and Instrumental Engineer, 1989 - 1995

- Worked for many factories and sections such as the Sugar Factory, the Electrical Workshop, the Power Generation Unit, and the Yeast Factory.
- Installed electrical panels and industrial machines such as electrical motors and automated centrifugal machines.
- Developed and installed control circuits such as temperature controllers and yeast cutting controller.
- Analyzed work orders and developed maintenance plans.

AWARDS AND GRANTS

- **2018-2019** two-year grant awarded by The Research Council of Oman Research Grant (RG) application under the Block Funding Program (BFP), Oman.
    - **PI, Sustained Water Desalination Station (SWDS)**
- **2018-2019** two-year grant awarded by The Research Council of Oman Research Grant (RG) application under the Block Funding Program (BFP), Oman.
    - **Co-Investigators,** Detection Techniques for Massive MIMO Systems: Enabling Technology of 5G
- **2015-2016** one-year grant awarded by The Research Council of Oman under the Faculty Mentored Undergraduate Research Award Program (FURAP), Oman.
    - **Mentor, Wireless Power Transmission**
- **2007:** One-year research grant awarded by the Department of Electrical and Computer Engineering, Ryerson University, Faculty Research Grants (FRG), Canada.
    - **Co-PI, FPGA platform for adaptive segmentation for nonstationary biomedical signals**

- **2006-2011:** Five-year research grant awarded by the Natural Science and Engineering Research Council of Canada (NSERC), Canada.
    - **PI, Modeling and Analyzing On-Chip Interconnect**
- **2005:** One-year research grant awarded by the Natural Science and Engineering Research Council of Canada (NSERC), Canada.
    - **PI, Design Reusability Driven Digital CMOS Circuit Design**
- **2004:** One-time research grant awarded by the Faculty of Engineering, Architecture and Science seed fund awarded by Ryerson University, Canada.
    - **PI, Seed fund**
- **1999 – 2001:** Two-year fellowship awarded by the Defense Research and Development Board (DRDB) of Canada.
    - **PI, Design Methodology for Intellectual Property (IP) blocks**

SERVICE TO THE PROFESSION

Associate Editor

- Recent Patents on Computer Science, *Bentham Science Publishers,* ***2010-2015***

Reviewer for

- IEEE Transactions on Electron Devices
- IEEE Transactions on Circuits and Systems-Part II
- IEEE Journal of Solid-State Circuits
- IEEE Transactions on Computer-Aided Design on Integrated Circuits and Systems
- IEE Proceedings Circuits, Devices & Systems
- IEEE International Midwest Symposium on Circuits and Systems
- IEEE International NEWCAS conference
- Canadian Conference on Electrical and Computer Engineering

PROFESSIONAL MEMBERSHIPS

- **Member,** Institute of Electrical and Electronics Engineers, **IEEE**
- **Member,** Professional Engineers of Ontario, **PEO** (Canada)

REFERENCES

Available upon request

PUBLICATIONS

PAPERS IN REFEREED JOURNALS

[1]. H. M. Shaik, **A. Kabbani,** A. M. Sheikh, Keng Goh, Naren Gupta, and T. Umar, "Measurement and validation of polysilicon photovoltaic module degradation rates over five years of field exposure in Oman" AIMS Energy, vol. 9, no. 6, pp. 1192-1212, 2021.

[2]. **A. Kabbani**, and M. S. Honnurvali, "PV Cell Parameters Modeling and Temperature Effect Analysis," *International Journal of Renewable Energy Development*, vol. 10 no. 3, pp. 563-571, 2021.

[3]. Mohamed Shaik Honnurvali; Naren Gupta; Keng Goh; Tariq Umar; **Adnan Kabbani**; Needa Nazeema, "Case study of PV output power degradation rates in Oman" *IET Renewable Power Generation*, vol. 13, no. 2, pp. 352 – 360, Feb. 2019.

[4]. **A. Kabbani,** "Optimum power supply for minimum energy in nano CMOS circuits," *Electrical Engineering*, Springer, vol. 99, no. 686, pp. 1-7, May 2017.

[5]. **A. Kabbani,** "Complex CMOS gate collapsing technique and its application to transition time," *Journal of Circuits, Systems and Computers*, vol. 19, no. 5, pp. 1025-1040, August 2010.

[6]. **A. Kabbani**, "Logical effort based dynamic power estimation and optimization of static CMOS circuits," *Integration, the VLSI Journal*, vol. 43, no. 3, pp. 279-288, June 2010.

[7]. B. Jiao, S. Krishnan, and **A. Kabbani**, "FPGA implementation of adaptive segmentation for nonstationary biomedical signals," *IEE Proceedings-Circuits Devices and Systems,* vol. 4, no. 3, pp. 239 – 250, May 2010.

[8]. D. Al-Khalili, H. El-Masry, **A. Kabbani** and J. Xue, "ASIC design paradigm based on a virtual-cell library," *International Journal of Computers, Information Technology and Engineering* (IJCITAE), vol. 1, no. 1, pp. 23-30, June.2007.

[9]. **A. Kabbani**, D. AlKhalili, A.J. Al-Khalili, "Technology portable analytical model for DSM CMOS inverter delay estimation" *IEE Proceedings-Circuits, Devices and Systems*, vol. 152, no. 5, pp. 433-440, Oct. 2005.

[10]. **A. Kabbani**, D. Al-Khalili, and A. J. Al-Khalili, "Delay Analysis of CMOS Gates Using Modified Logical Effort Model," *IEEE transactions on Computer-Aided Design on Integrated Circuits and Systems,* vol. 24, no. 6, pp. 937-947, June. 2005.

[11]. **A. Kabbani**, D. Al-Khalili, and A. J. Al-Khalili, "Technology-portable analytical model for DSM CMOS inverter transition time estimation," *IEEE transactions on Computer-Aided Design on Integrated Circuits and Systems,* vol. 22, no. 9, pp. 1177-1187, Sept. 2003.

[12]. **A. Kabbani** and A. J. Al-Khalili, "Technique for dynamic CMOS noise immunity evaluation," *IEEE transactions on Circuits and Systems-I: fundamental Theory and Application*, vol. 50, no. 1, pp. 74-87, Jan. 2003.

[13]. **A. Kabbani** and A. J. Al-Khalili, "Estimation of ground bounce effects on CMOS circuits," *IEEE transactions on Component and Packaging Technology, Part 1,* vol., 22, no. 2, pp. 316-325, June 1999.

PAPERS IN REFEREED CONFERENCE PROCEEDINGS

[14]. Mohamed Shaik Honnurvali, Naren Gupta, Keng Goh, **Adnan Kabbani**, Tariq Umar, Needa Nazeema, "Can future smart cities powered by 100% renewables and made cyber secured an Analytical Approach," 12th *International Conference on Global Security, Safety & Sustainability*, London, 2018.

[15]. M.S.N Vali, **A. Kabbani**, and N. Nazeema, "Millimeter wave Propagation Measurements in Forest for 5G Wireless Sensor Communications," *Proceedings of the 16th IEEE-Mediterranean Microwave Symposium*, Nov. 2016.

[16]. A. Abdullah, **A. Kabbani** and K. Raahemifar, "Mapping the AWE-RLC model into a simple RC circuit with its application to buffer insertion," *Proceedings of Canadian Conference on Electrical and Computer Engineering*, pp. 152-155, 2011.

[17]. B. Jiao, S. Krishnan, and **A. Kabbani**, "FPGA implementation of AR modeling based on Burg algorithm " *accepted in BRC2010,* Jan. 2010.

[18]. **A. Kabbani**, "Transistor sizing and VDD scaling for low power CMOS circuits," *IEEE Northeast Workshop on Circuits and Systems*, pp. 1-4, June-July 2009.

[19]. M. Pullerits, and **A. Kabbani**, "Area Minimization for Library-Free Synthesis," *IEEE Northeast Workshop on Circuits and Systems*, pp. 1-4, June –July, 2009.

[20]. M. Pullerits, and A**. Kabbani**, "Library-free synthesis for area-delay minimization," *proceedings of the 20th International Conference on Microelectronics*, pp. 162-166, Dec. 2008.

[21]. **A. Kabbani**, "Modeling and optimization of switching power dissipation in static CMOS circuits," *proceedings of IEEE Computer Society Annual Symposium on VLSI*, pp. 281-285, Apr. 2008.

[22]. D. Al-Khalili, H. El-Masry, **A. Kabbani**, and J. Xue, "Virtual-cell library based paradigm in ASICs yield custom performance," *proceeding of the 3rd International Conference on Computers and Devices for Communication*, Dec. 2006.

[23]. **A. Kabbani**, D. Al-Khalili, and A. J. Al-Khalili, "Logical path delay distribution and transistor sizing," *proceedings of the third IEEE Northeast Workshop on Circuits and Systems*, pp. 391-394, June 2005.

[24]. **A. Kabbani**, D. Al-Khalili, A.J. Al-Khalili, "Delay Macro Modeling of CMOS Gates Using Modified Logical Effort Technique," *proceedings of IEEE Conference on Semiconductor Electronics*, pp. 56-60. 2005.

[25]. **A. Kabbani**, D. Al-Khalili, and A. J. Al-Khalili, "Technology Portable Delay Model for DSM CMOS Inverters," *proceedings of the second IEEE Northeast Workshop on Circuits and Systems*, pp. 13-16, June 2004.

[26]. **A. Kabbani**, D. Al-Khalili, and A. J. Al-Khalili, "Technology-portable analytical model for DSM CMOS inverter transition time estimation," *proceedings of the 46th IEEE Midwest Symposium on Circuits and Systems, pp.* 1463-1468, Dec. 2003.

[27]. **A. Kabbani** and A. J. Al-Khalili, "Dynamic CMOS noise immunity estimation in submicron regime," *proceedings of IEEE International Symposium on Circuits and Systems*, pp. 529-532, May 1999.

[28]. **A. Kabbani** and A. J. Al-Khalili, "Estimation of Ground Bounce Effects on CMOS Circuits," *proceedings of IEEE International Symposium on Circuits and Systems*, pp. 533-536, May 1999.

[29]. **A. Kabbani** and A. J. Al-Khalili, "Noise immunity in dynamic CMOS circuits," *proceedings of the 10th International Conference on Microelectronics*, pp.41-44, Dec. 1998.

OTHER PAPERS

- **A. Kabbani, "**System-on-chip memory integration", *CMC Newsletter on Canada's System-On-Chip Research Network*, vol. 1, no. 3, May 14, 2003.
- **A. Kabbani, "**A Systematic Approach to Soft IP Block Authoring", *CMC Newsletter on Canada's System-On-Chip Research Network*, vol. 1, no. 2, Dec. 4, 2002.